REMARKS

In the Drawings

The Examiner objected to the drawings under 37 C.F.R. § 1.83(a). The Examiner states that the drawings do not show the limitation in claim 31 of "the spacers that are recessed to lower surface of the conductive layer." This language occurred at four locations in claim 31, and has been deleted at all four locations. As such, Applicant respectfully requests withdrawal of the objections to the drawings under 37 C.F.R. § 1.83(a).

Rejection of Claims Under 35 U.S.C. § 112

The Examiner has rejected claims 31-39 under 35 U.S.C. § 112, first paragraph and second paragraph. The Examiner's rejections appear to relate to the language of "the spacers that are recessed to lower surface of said conductive layer," which has been deleted.

Applicant, accordingly, respectfully requests withdrawal of the rejections of 31-39 under 35 U.S.C. § 112, first paragraph and second paragraph.

Rejection of Claims Under 35 U.S.C. § 103

The Examiner rejected claims 31-39 under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto. The Examiner states that it has been held that mere duplication of parts has no patentable significance unless a new or unexpected result is produced (Page 4, lines 5-7). The advantage of having

multiple spacers is that the spacers can be individually etched as illustrated in Figures 6I, 6J, 6L, and 6M respectively. Such individual etching allows for tailoring of spacers having specific thicknesses and heights, and being made of specific materials.

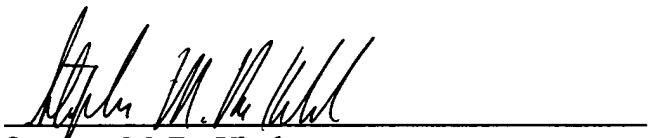
Applicant has thus demonstrated that a new and unexpected result is produced. Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 31-39 under 35 U.S.C. § 103(a) in view of Matsumoto.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: August 12, 2002



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VERSION OF CLAIMS WITH MARKINGS

31. (Twice Amended) A gate electrode comprising:

an insulative layer disposed on a substrate;

a gate layer disposed on said insulative layer;

[a conductive layer disposed on said gate layer, said conductive layer extending beyond edges of said gate layer;]

thin first spacers disposed adjacent to opposite sides of said gate layer [wherein said thin first spacers are recessed to lower surface of said conductive layer];

thin second spacers disposed adjacent to opposite sides of said thin first spacers [wherein said thin second spacers are recessed to lower surface of said conductive layer];

thin third spacers disposed adjacent to opposite sides of said thin second spacers [wherein said thin third spacers are recessed to lower surface of said conductive layer]; [and]

thick fourth spacers disposed adjacent to opposite sides of said thin third spacers [wherein said thick fourth spacers are recessed to lower surface of said conductive layer]; and

a conductive layer disposed on said gate layer, extending beyond edges of said gate layer and having a lower side at least as high as upper edges of said first, second, third, and fourth spacers.